APPENDIX

1. A voltage divider system (102), comprising:

a high voltage impedance element (104), connected to an input node for receiving an input signal;

a low voltage impedance element (106), connected to the high voltage impedance element (104); ~~and~~

at least one guard element (118), the at least one guard element (118) being coupled between the high voltage impedance element (104) and ground.;

wherein the at least one guard element (118) comprises at least one capacitive element; and

wherein the at least one guard element (118) further comprises at least one resistive guard element (124) coupled to the at least one capacitive element.

9. The system of claim ~~8~~ 1, wherein the at least one capacitive element comprises at least one capacitor.

14. The system of claim ~~13~~ 1, wherein the at least one resistive guard element (124) comprises at least one resistor coupled to the at least one capacitive element.

15. The system of claim ~~13~~ 1, wherein the at least one resistive guard element (124) increases a stability of a voltage drop across the high voltage impedance element (104).

19. A method for processing a signal, comprising:

a) receiving an input signal via an input node (108) connected to a high voltage impedance element (104);

b) communicating a reduced voltage representation of the input signal from the high voltage impedance element (104) to a low voltage impedance element (106); ~~and~~

c) coupling at least one guard element (118) between the high voltage impedance element (104) and ground~~.~~;

wherein the guard element (118) comprises at least one capacitive element; and

wherein the at least one guard element (118) further comprises at least one resistive guard element (124), further comprising a step of d) coupling the at least one resistive guard element (124) to the at least one capacitive element.

20. The method of claim 19, further comprising a step of ~~d)~~ e) sampling the reduced voltage representation of the input signal at a sample node (110) between the high voltage impedance element (104) and the low voltage impedance element (106).

21. The method of claim 20, further comprising a step of ~~e)~~ f) connecting a measurement device (116) to the sample node (110) to perform the sampling.

22. The method of claim 21, further comprising of a step ~~f)~~ g) sampling at least one of voltage, current, frequency, and phase in the measurement device (116).

27. The method of claim ~~26~~ 19, wherein the at least one capacitive element comprises at least one capacitor.

32. The method of claim ~~31~~ 19, wherein the at least one resistive guard element (124) comprises at least one resistor coupled to the at least one capacitive element.

33. The method of claim ~~32~~ 19, wherein the at least one resistive guard element (124) increases a stability of a voltage drop across the high voltage impedance element (104).

37. A voltage divider system, comprising:

high voltage impedance means (104), connected to an input node for receiving an input signal;

low voltage impedance means (106), connected to the high voltage impedance means (104); ~~and~~

at least one guard means (118), the at least one guard means (118) being coupled between the high voltage impedance means (104) and ground~~.~~;

wherein the at least one guard means (118) comprises at least one capacitive element; and

wherein the at least one guard means (118) further comprises at least one resistive guard means (124) coupled to the at least one capacitive element.

45. The system of claim ~~34~~ 37, wherein the at least one capacitive element comprises at least one capacitor.

50. The system of claim ~~49~~ 37, wherein the at least one resistive guard means comprises at least one resistor coupled to the at least one capacitive ~~means~~ element.

51. The system of claim ~~49~~ 37, wherein the at least one resistive guard means (124) increases a stability of a voltage drop across the high voltage impedance element (104).

55. A voltage divider (102), comprising:

a plurality of series-connected high voltage resistors (114a, 114b ... 114n), the series-connected high voltage resistors (114a, 114b ... 114n) connected to an input node (110) for receiving an input signal;

at least one low voltage resistive element (106), the at least one low voltage resistive element (106) connected to the series-connected high voltage resistors (114a, 114b ... 114n); ~~and~~

at least one capacitive guard (118), the at least one capacitive guard (118) connected between the series-connected high voltage resistors (114a, 114b ... 114n) and ground~~.~~; and

wherein the at least one capacitive guard (118) further comprises at least one resistive guard (124) coupled to the at least one capacitive guard (118).

60. The voltage divider of claim ~~59~~ 55, wherein the at least one resistive guard (124) comprises at least one resistor coupled to the at least one capacitive guard (118).

61. The voltage divider of claim ~~59~~ 55, wherein the at least one resistive guard (124) increases a stability of a voltage drop across the series-connected high voltage resistors (114a, 114b ... 114n).